WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory comprising:

a memory cell;

a bit line connected to one end of the memory cell; and

a data circuit which is connected to the bit line and in which program data or read data concerning the memory cell is temporarily stored,

wherein the data circuit includes: first, second, and third data storage units; a first data transfer circuit connected between the first and third data storage units; and a second data transfer circuit connected between the second and third data storage units, and

the first data storage unit is connected to the bit line, and the second data storage unit includes a function of forcibly changing data of the first data storage unit based on the data stored in the second data storage unit.

2. A nonvolatile semiconductor memory according to claim 1, wherein the first and second data storage units are constituted of capacitors.

3. A nonvolatile semiconductor memory according to claim 1, wherein the first data storage unit is constituted of a MOS capacitor.

4. A nonvolatile semiconductor memory according to claim 1, wherein the second data storage unit is

constituted of a MOS transistor whose gate is connected to the second data transfer circuit, and a third data transfer circuit is connected between a drain of the MOS transistor and the first data storage unit.

5. A nonvolatile semiconductor memory according to claim 1, wherein the third data storage unit is constituted of a latch circuit.

6. A nonvolatile semiconductor memory according to claim 5, wherein the latch circuit is constituted of a CMOS flip-flop circuit.

7. A nonvolatile semiconductor memory according to claim 4, wherein the data circuit further includes: a fourth data storage unit connected to a data line via a column selection switch; and a fourth data transfer circuit connected between the first and fourth data storage units.

8. A nonvolatile semiconductor memory according to claim 7, wherein the fourth data storage unit is constituted of a latch circuit.

9. A nonvolatile semiconductor memory according to claim 8, wherein the latch circuit is constituted of a CMOS flip-flop circuit.

10. A nonvolatile semiconductor memory according to claim 1, wherein the data circuit further includes: a clamp circuit connected between the bit line and first data storage unit; and a precharge circuit connected to the first data storage unit.

11. A nonvolatile semiconductor memory according to claim 1, further comprising: a detection circuit which judges presence/absence of completion of a program with respect to the memory cell based on the data stored in the third data storage unit.

12. A nonvolatile semiconductor memory according to claim 1, wherein the first and second data transfer circuits are constituted of MOS transistors.

13. A nonvolatile semiconductor memory according to claim 7, wherein the third and fourth data transfer circuits are constituted of MOS transistors.

14. A nonvolatile semiconductor memory according to claim 1, wherein the memory cell stores two bits or more data.

15. A nonvolatile semiconductor memory according to claim 1, wherein the memory cell is a nonvolatile memory cell including a floating gate electrode and control gate electrode.

16. A nonvolatile semiconductor memory according to claim 7, further comprising: a control circuit which controls movement of the read data in the data circuit.

17. A nonvolatile semiconductor memory according to claim 16, wherein with respect to the memory cell which has four states, the control circuit includes: means for storing first read data read from the memory cell at a first read potential into the third data storage unit; means for transferring the first read

data to the second data storage unit from the third data storage unit; means for storing second read data read from the memory cell at a second read potential into the first data storage unit; means for forcibly changing a value of the second read data stored in the first data storage unit based on the first read data stored in the second data storage unit; and means for transferring the second read data to the fourth data storage unit from the first data storage unit.

18. A nonvolatile semiconductor memory according to claim 7, further comprising: a control circuit which controls movement of the program data in the data circuit.

19. A nonvolatile semiconductor memory according to claim 18, wherein the control circuit includes: means for storing the program data into the fourth data storage unit; means for transferring the program data to the third data storage unit from the fourth data storage unit; and means for transferring the program data to the second data storage unit from the third data storage unit.

20. A nonvolatile semiconductor memory according to claim 19, wherein with respect to the memory cell which has a function of storing two bit data and in which one bit data of the data is already stored, the control circuit includes: means for transferring the program data to the third data storage unit from the

fourth data storage unit and subsequently resetting a state of the fourth data storage unit; and means for reading the one bit data stored in the memory cell into the fourth data storage unit.

21. A nonvolatile semiconductor memory according to claim 19, wherein the control circuit includes means for determining whether or not the threshold voltage of the memory cell is fluctuated based on the value of the program data stored in the third data storage unit at a write operation time.

22. A nonvolatile semiconductor memory according to claim 21, wherein the value of the program data stored in the third data storage unit is changed in accordance with the data read from the memory cell by verify read.

23. A nonvolatile semiconductor memory according to claim 22, wherein the value of the program data stored in the second data storage unit does not always change.

24. A nonvolatile semiconductor memory according to claim 23, wherein the control circuit includes: means for resetting a state of the third data storage unit after completion of programming with respect to the memory cell; and means for transferring the program data stored in the second data storage unit to the third data storage unit.

25. A nonvolatile semiconductor memory according

to claim 1, wherein for the program data stored in the second and third data storage units, in order to determine whether or not the threshold voltage of the memory cell is fluctuated based on the value of the program data stored in the third data storage unit at a write operation time, the control circuit includes: means for storing the read data into the first data storage unit by verify read; means for forcibly changing the value of the read data stored in the first data storage unit in accordance with the value of the program data stored in the second data storage unit; and means for storing the read data stored in the first data storage unit as the program data into the third data storage unit.

26. A nonvolatile semiconductor memory according to claim 20, wherein the control circuit includes: means for storing the read data into the first data storage unit by verify read; means for forcibly changing the value of the read data stored in the first data storage unit in accordance with the value of the one bit data stored in the fourth data storage unit; and means for storing the read data stored in the first data storage unit as the program data into the third data storage unit.

27. A nonvolatile semiconductor memory comprising:

a nonvolatile semiconductor memory cell which can electrically be rewritten;

a bit line connected to the memory cell;

a read circuit which reads out data of the memory cell and which includes a first data storage unit connected to the bit line, a second data storage unit having a function of forcibly changing the data of the first data storage unit in accordance with the data stored in the second data storage unit, a third data storage unit having a function of reading out the data of the first data storage unit, and a data transfer circuit to transfer the data of the third data storage unit to the second data storage unit; and

a read control circuit which reads the data of the memory cell into the first data storage unit via the bit line, forcibly changes the read data of the first data storage unit in accordance with the data of the second data storage unit, subsequently transfers the data of the third data storage unit to the second data storage unit, and further subsequently reads out the data of the first data storage unit by the third data storage unit.

28. A nonvolatile semiconductor memory according to claim 27, wherein the first and second data storage units accumulate electric charges into capacitors to store the data.

29. A nonvolatile semiconductor memory according to claim 28, wherein the data transfer circuit is constituted of a first MOS transistor, the second data

storage unit is constituted of a second MOS transistor, a source of the second MOS transistor is connected to a first electrode of a capacitor of the first data storage unit via a third MOS transistor, and a gate of the second MOS transistor is connected to the source of the first MOS transistor.

30. A nonvolatile semiconductor memory according to claim 29, wherein the third data storage unit is constituted of two CMOS flip-flops, connected to a drain of the first MOS transistor, and further connected to the first electrode of the capacitor of the first data storage unit via a fourth MOS transistor.